A Gain-Adaptive Column Amplifier for Wide-Dynamic-Range CMOS Image Sensors

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Abstract—**A robust gain-adaptive column amplifier scheme which is friendly to the digital correlated multiple sampling (DCMS) A/D conversion is proposed to extend the dynamic range of CMOS image sensors. It lowers the noise at low light levels and relaxes the gain to prevent saturation at high light levels, while a low-noise readout circuit is not necessary because of the dominance of photon shot noise. Since the difference between the reset and the signal levels at a 4T pixel output is compared with reference voltages to detect the suitable gain values, the fixed pattern noise (FPN) caused by this gain detection scheme is estimated to be 20 times lower than that of the work in which only the pixel signal level is compared. Operation analysis and Monte-Carlo simulations show the immunity of the circuit to unwanted offsets. Noise analysis and SNR calculation show that the FPN by the gain-detection scheme is more suppressed with either more gain options or the DCMS conversion applied at the amplifier output. A column-level design with a size of *9μm×500μm* and a current consumption of *12μA* is discussed to demonstrate the feasibility of the idea.**

***Index Terms*—Gain-adaptive amplifier, CDS comparison, digital correlated multiple sampling, wide dynamic range image sensors, fixed pattern noise.**

I. Introduction

IN CMOS image sensors, many extended dynamic range (DR) techniques have been proposed in order to reach the human eye limit, which exceeds 90dB of dynamic range [3]. Some pixel-level DR extension techniques [3] widen the upper limit for high illuminations by increasing the maximum pixel current. However, all of these techniques have a pixel complication disadvantage associated with the pixel-level processing. Therefore, these pixels tend to be larger and noisier than conventional ones. Fig. 1 shows a column-level DR extension principle based on the adaptive readout noise characteristic, in which the gain is adaptively changed among the low, medium and high values according to the illumination ranges. Since, at the high illumination range, the noise is dominated by photon shot noise [1], which is proportional to the square root of the light intensity, a low-noise readout is not needed, and the gain can be relaxed to prevent the circuits from saturation. As a result, the DR is extended towards the low illumination range, where a high gain is applied. A similar technique but with an adaptive quantization noise approach was discussed by Theuwissen [2].

A gain-adaptive column amplifier [4] has been proposed to extend the dynamic range based on the adaptive read noise behavior in Fig. 1. In this method, where the gain assessment is made prior to the actual amplification [4], there is a disadvantage that the comparator detects the gain level in the signal-level readout phase, which contains both the reset noise level and the offsets of the pixel. Therefore, the comparison introduces errors to cause a fixed pattern noise (FPN) within the threshold voltage border range, in which, for the same pixel output level, the gains are differently set to high or low among columns. This gain-uncertainty range is mainly contributed by the un-cancelled pixel offset in the gain detection phase. In addition, the threshold voltage has to be adjusted a little lower than the expected value to prevent saturation by such unpredictable offsets. Furthermore, this scheme is not appropriate for high-gain detection applications, where small input ranges are detected and highly accurate comparisons are required.

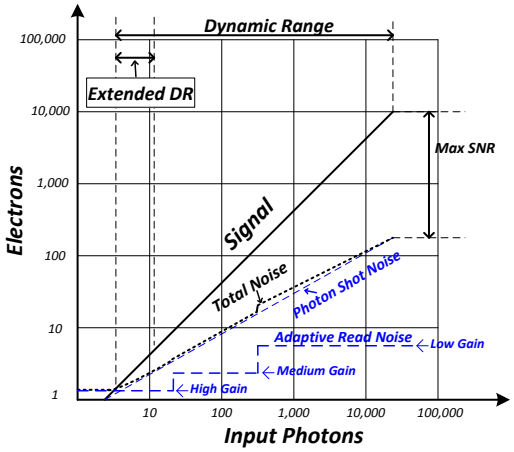

Fig. 1. Photon conversion characteristics: the gain and hence the readout noise floor is adaptively changed over the illumination range.

In this paper, a robust gain-adaptive amplifier is proposed in Section II, which solves the problems of the above amplifier. Section III presents the noise analysis and practical issues of a 4T pixel gain-adaptive column readout chain.

II. The Proposed Gain-Adaptive Amplifier

Fig. 2 (a) shows the schematic of the proposed gain-adaptive column amplifier. The work is based on the correlated double sampling (CDS) readout operation, in which the pixel is read out twice, once right after the pixel reset (called the reset-level readout phase), and secondly after the end of the pixel integration (called the signal-level readout phase) [3]. This CDS operation helps to remove the fixed pattern noise (FPN) and the reset noise of the pixel. The node *INPUT* represents the CDS behavior for the output of a 4T pixel. Fig. 2(b) shows the timing diagram of the circuit in Fig. 2 (a) in one complete CDS pixel readout period. For the sake

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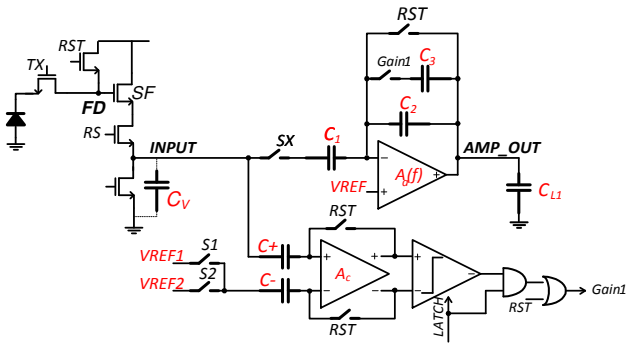
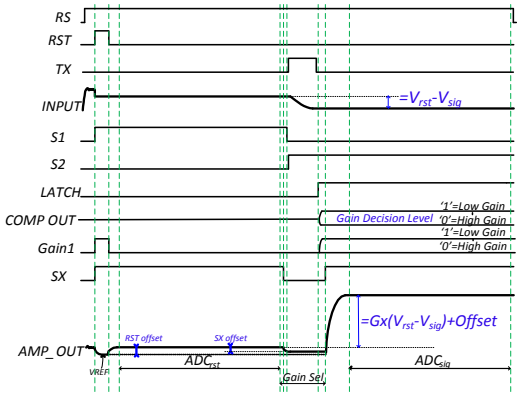
of illustration, a two-gain option of 1 and 8 is shown. This principle, however, can be extended to more gain levels as shown in Fig. 1 by adding extra reference levels and D-flipflops to store the comparison results. Then, more latch periods are needed, but the extra time can be minimized by designing a fast comparator. In this work, the amplifier is designed as a closed-loop capacitive structure which works in three operating phases: the reset-level readout phase, the gain detection phase, and the signal-level readout phase. Therefore, this scheme is very friendly to the digital correlated multiple sampling (DCMS) conversion [7], [8], in which not only is the vertical fixed pattern noise (VFPN) among columns cancelled, but the readout thermal noise is also suppressed. In Fig. 2 (a), there is an additional switch *SX* at the input capacitor C_1 to isolate the node *INPUT* and the amplifier input during the gain detection phase [4]. Firstly, both the amplifier and the comparator are reset. Then, when the reset switch *RST* disconnects, the amplifier works in the reset-level readout phase with the default maximum gain value G_{max}. As a consequence and shown in Fig. 2 (b), this *RST* discharging operation causes an offset voltage V_{RST_offset} at the amplifier output *AMP_OUT*. This offset voltage stays there for the whole readout period and is finally cancelled by the CDS.



(a)



(b)

Fig. 2. (a) Schematic of the proposed gain-adaptive column amplifier; (b) timing diagram of the 4T pixel and the proposed amplifier.

When the reset-level readout phase is finished, the amplifier changes to the gain detection phase by disconnecting the switch *SX*. Then, the CDS input level $(V_{rst}\text{-}V_{sig})$ at the capacitor *C+* is compared with the shifted reference level *(VREF1-VREF2)* at the capacitor *C-*, and the gain value is detected right after the *LATCH* rising edge. Then, shortly after that, *SX* re-connects, and the amplifier is changed into the signal-level readout phase, when the pixel output has been shifted from V_{rst} to V_{sig}. Ideally, the amplifier output *AMP_OUT* is accordingly changed by an amount of $G\times(V_{rst}\text{-}V_{sig})$, where *G* is the detected gain. In this example, *G* is 1 or 8.

However, the SX switching-off action at the beginning of the gain detection phase injects an offset $V_{SX\_injected}$ onto the amplifier capacitor C_1, and the amplifier output is shifted by an amount of $V_{SX\_offset}=-8\times V_{SX\_injected}$ because the gain is set to the default value of 8 at the moment. This offset value V_{SX_offset} stays there for the whole CDS operation. In the signal-level readout phase when the switch *SX* is reconnected, there is a change from $(V_{rst}+ V_{SX\_injected})$ to V_{sig} at the amplifier input, thus the amplifier output is then shifted from the value in the reset-level readout phase by an amount of

$$G(V_{rst}\text{-}V_{sig})+(G\text{-}8)V_{SX\_injected} \quad (1).$$

From (1), it can be realized that, for the gain of 8, there is no residual offset, while for a gain of 1, the offset value is $-7\times V_{SX\_injected}$. Thus, only the large input signal is affected by this offset, whose value and variation decrease as the size of the input capacitor C_1 increases. On the other hand, since the offset voltage can be subtracted afterwards, only the offset variation causes the FPN among columns. However, the Monte-Carlo simulation result indicates that the standard variation of the offset value is $400\mu V$ for the gain options of 1 and 8. Such a value is 8 times lower than the photon shot noise at the input signal of *125mV* (assume that the full input swing is *1V* and the pixel conversion gain is $80\mu V/e^-$). When the gain increases, the threshold voltage decreases accordingly; however, the input capacitor C_1 of the amplifier is proportionally sized up. As a result, such an offset variation is suppressed and its impact on the performance remains little.

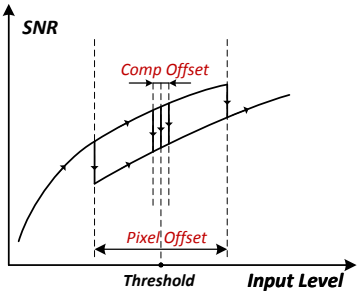


Fig.3 SNR drop point variations in the threshold border range.

As shown in Fig. 3, because of the gain-adaptive behavior, there is a SNR drop when the input level moves from the lower to the higher range of the threshold voltage. Ideally, such a SNR shift happens only at the threshold voltage. However, due to the pixel and the comparator offset, the SNR drop point varies from column to column, especially in the technique proposed by Sakakibara [4], in which only the V_{sig} level of the node *INPUT* is compared with the threshold voltage to detect the gain value. This scheme suffers from the reset noise and especially from the pixel offset caused by the temperature and process variations. As a result, the range of the SNR uncertainty, which raises the FPN issue, is dominated by the variation of the level V_{sig}. However, with the proposed technique, since the CDS input level $(V_{rst}\text{-}V_{sig})$ is compared with the reference levels *(VREF1-VREF2)*, this FPN range is mainly contributed by the comparator offset, which can reach to lower *1mV* range by auto-zeroing operation instead of a

20mV pixel offset range (assume pixel FPN of 2% with a full range of *1V*). A smaller range of SNR uncertainty means a lower probability of FPN, therefore, with the proposed technique, the columns are estimated to be 20 times more free from the FPN caused by the gain detection phase. The higher the values of the input capacitors *C+* and *C-*, and the pre-amplifier gain A_c, the more precise the comparator is [5]. In addition, either of the two references *VREF1* and *VREF2* can reuse the reference voltage *VREF* of the amplifier because the switches S_1 and S_2 alter just once in the whole readout period.

III. Noise Analysis And Practical Issues

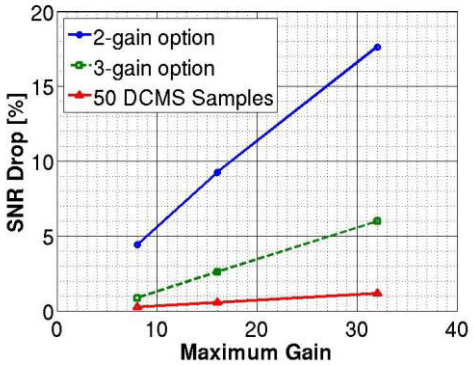


Fig. 4 SNR drop over the maximum gain value of the gain-adaptive amplifier for three cases: two-gain option, three-gain option, and 50 DCMS samples.

Since the *1/f* noise is high-pass filtered out by the CDS operation [7], we will now analyze the thermal noise performance of a column-level readout chain as described in Fig. 2 (a). Based on the thermal noise equations developed by Kawahito [6] and Chen [8] for the 4T pixel readout circuit, the total thermal input-referred noise at the node *INPUT* in both the reset-level readout phase and the signal-level readout phase can be expressed as:

$$\overline{V_{n,INPUT}^2} = \left(\frac{1}{1+G_{max}} + \frac{1}{1+G}\right)\frac{F_{SF}^2 \xi_{SF} k_B T}{C_{L1}}\frac{gm_a}{gm_{SF}} + 2\frac{k_B T}{C_1} + \left(\frac{1+G_{max}}{G_{max}^2} + \frac{1+G}{G^2}\right)\frac{\xi_a k_B T}{C_{L1}} \quad (2)$$

where k_B is Boltzman's constant, T is the absolute temperature, C_V is the column parasitic capacitance, C_1 and C_{L1} are respectively the input and the output capacitances of the amplifier, gm_a and gm_{SF} are the transconductances of the amplifier and the pixel source follower, respectively. F_{SF} and ξ_{SF} are the noise gain factor and the excess noise factor of the source follower [6], [8], ξ_a is the excess noise factor of the amplifier, G_{max} is the maximum gain of the amplifier, G is the detected gain value in the signal-level readout phase.

Based on equation (2), it can be seen that there is a noise shift when the CDS input level $(V_{rst}\text{-}V_{sig})$ goes from the lower to the higher range of the threshold voltage *(VREF1-VREF2)*. The larger such a noise shift is, the more the SNR will drop. As a result, the FPN caused by the gain-detection comparison described in Fig. 3 increases. Fig. 4 shows the SNR drop percentage over the maximum gain value of the proposed gain-adaptive amplifier for three cases: two-gain option, three-gain option, and two-gain option with 50 DCMS samples applied at the amplifier output. The calculations are based on equation (2) and the value assumptions in Kawahito's work [6] and Chae'work [7]. For the case of two-gain option (*1*, G_{max}), SNR is shown to drop more as the maximum gain increases. If three gain options are used, the SNR drop is reduced but at the cost of the system complication. If the DCMS conversion like a 2nd-order incremental sigma delta (ISD) ADC [7] with 50 samples is applied at the amplifier output, the thermal noise is averaged. As the result, the SNR drop is strongly suppressed, and hence so be the FPN.

For the area and power estimations, the full schematic design and layout of a gain-adaptive column amplifier are done to verify the design feasibility. For the maximum gain of 8, the gain-adaptive column amplifier occupies a size of $9\mu m \times 500\mu m$ and consumes a static current of $12\mu A$, while the output settling time at the beginning of the signal-level readout phase in Fig. 2 (b) is less than *400ns*. In order to drive a large load like an ISD ADC, a high current buffer is needed at the amplifier output, which increases considerably the size and the power of the design, depending on the sampling frequency.

IV. Conclusions

This paper has presented a robust gain-adaptive column amplifier for CMOS image sensors. This amplifier detects the appropriate gain by implementing the CDS operation at the comparator to compare the $(V_{rst}\text{-}V_{sig})$ value with the difference of the two reference values. This approach shows advantages of being fast, accurate, and robust over process and temperature variations. Compared to the previous work [4], in this design, the FPN by the gain detection comparison is reduced from the pixel offset range, which can not be controlled, to the comparator offset range, which is strongly suppressed by the auto-zeroing operation. Noise analysis has shown that the above FPN is more suppressed with either more gain options or the DCMS conversion like an ISD ADC applied at the amplifier output. Some practical issues have been discussed to show the feasibility of the design.

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